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(54) **SEMICONDUCTOR PACKAGE AND METHOD FOR FABRICATING THE SAME**

(75) Inventors: **WonSun Shin**, Kyungki-do (KR);
DoSung Chun, The Kingdom of
Thailand (TH); **SangHo Lee**, Seoul
(KR); **SeonGoo Lee**, Kyungki-do (KR);
Vincent DiCaprio, Mesa, AZ (US)

(73) Assignee: **Amkor Technology, Inc.**, Chandler, AZ
(US)

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(56) **References Cited**

U.S. PATENT DOCUMENTS

3,851,221 A 11/1974 Beaulieu et al. 317/100
4,530,152 A 7/1985 Roche et al. 29/588

(List continued on next page.)

FOREIGN PATENT DOCUMENTS

EP 503 201 A2 12/1991 H01L/23/495
JP 54-128274 4/1979 H01L/23/30

JP	56-062351	5/1981	H01L/25/04
JP	60-182731	9/1985	H01L/21/60
JP	61-059862	3/1986	H01L/25/04
JP	61-117858	6/1986	H01L/25/08
JP	62-119952	6/1987	H01L/25/04
JP	62-126661	6/1987	H01L/25/04
JP	62-142341	6/1987	H01L/25/04
JP	63-128736	6/1988	H01L/23/04
JP	63-211663	9/1988	H01L/25/08
JP	63-244654	10/1988	H01L/23/28
JP	10-28856	1/1989	H01L/27/00

(List continued on next page.)

Primary Examiner—Charles Bowers

Assistant Examiner—Chuong Anh Luu

(57) **ABSTRACT**

Semiconductor packages having a thin structure capable of easily discharging heat from a semiconductor chip included therein, and methods for fabricating such semiconductor packages, are disclosed. An embodiment of a semiconductor package includes a semiconductor chip having a first major surface and a second major surface, the semiconductor chip being provided at the second major surface with a plurality of input/output pads; a circuit board including a resin substrate having a first major surface and a second major surface, a first circuit pattern formed at the first major surface and provided with a plurality of ball lands, a second circuit pattern formed at the second major surface and provided with a plurality of bond fingers connected with the ball lands by conductive via holes through the resin substrate, cover coats respectively coating the first and second circuit patterns while allowing the bond fingers and the ball lands to be exposed therethrough, and a central through hole adapted to receive the semiconductor chip therein; electrical conductors that electrically connect the input/output pads of the semiconductor chip with the bond fingers of the circuit board, respectively; a resin encapsulate that covers the semiconductor chip, the electrical conductors, and at least part of the circuit board; and, a plurality of conductive balls fused on the ball lands of the circuit board, respectively.

35 Claims, 15 Drawing Sheets

